AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor device having a System in Package structure in which a system comprises:

a wiring substrate;

a microcomputer chip; and

a memory chip, said microcomputer chip and said memory chip being mounted over ~~the~~ an upper surface of said wiring substrate, and

wherein said microcomputer chip is constructed ~~of~~ as a multiport device ~~structure~~ including an interface between ~~it~~ said microcomputer chip and ~~the~~ another part ~~inside~~ of said system including said memory chip and an interface between ~~it~~ said microcomputer chip and ~~the~~ outside of said system, ~~respectively,~~

wherein said memory chip is constructed ~~so as~~ to be accessed ~~to~~ from the outside of said system via said microcomputer chip, ~~and~~

wherein said microcomputer chip has a substantially square planar shape,

wherein said memory chip has a substantially rectangular planar shape,

wherein a length of a side of said microcomputer chip is shorter than a length of a long side of said memory chip, and

wherein said microcomputer chip is mounted over said wiring substrate in a state being stacked over said memory chip.

2. (currently amended) The semiconductor device according to claim 1, wherein said microcomputer chip is connected to first electrodes of said wiring substrate via a plurality of bonding wires, said memory chip is connected to second electrodes of said wiring substrate via a plurality of bonding wires or a plurality of bump electrodes, and said first electrodes are arranged ~~at the~~ toward an outer periphery ~~side~~ of said wiring substrate from said second electrodes.

3. (currently amended) The semiconductor device according to claim 1, wherein said memory chip ~~is formed with~~ includes a DRAM or a flash memory.

Claims 4-5 (cancelled).

6. (currently amended) A semiconductor device having a System in Package structure in which a system ~~is constituted of~~ comprises:

a wiring substrate;

~~one~~ a microcomputer chip; and

two memory chips, said microcomputer and said memory chips being mounted over ~~the~~ an upper surface of said wiring substrate, and

wherein said microcomputer chip is constructed ~~of~~ as a multiport device ~~structure~~ including an interface between ~~it~~ said microcomputer chip and ~~the~~ another part ~~inside~~ of said system including said two memory chips and an interface between ~~it~~ said microcomputer chip and ~~the~~ outside of said system, ~~respectively,~~

wherein each of said two memory chips is constructed ~~so as~~ to be accessed ~~to~~ from the outside of said system via said microcomputer chip, ~~and~~

wherein said microcomputer chip has a substantially square planar shape,

wherein each of said memory chips has a substantially rectangular planar shape,

wherein a length of a side of said microcomputer chip is shorter than a length of a long side of each of said two memory chips, and

wherein said two memory chips are mounted over said wiring substrate in a state ~~that~~ in which one of ~~them~~ said memory chips is stacked over the other and said microcomputer chip is mounted over said wiring substrate in a state of being stacked over said two memory chips.

7. (currently amended) The semiconductor device according to claim 6, wherein said microcomputer chip is connected to first electrodes of said wiring substrate via a plurality of bonding wires, ~~the~~ a lower memory chip ~~as the lower layer~~ of said two memory chips is connected to second electrodes of said wiring substrate via a plurality of bump electrodes, ~~the~~ an upper memory chip ~~as the upper layer thereof~~ of said two memory chips is connected to third electrodes of said wiring substrate via a plurality of bonding wires, and said first electrodes are arranged ~~at the~~ toward an outer periphery ~~side~~ of said wiring substrate from said second and third electrodes.

8. (currently amended) The semiconductor device according to claim 6, wherein one of said two memory chips ~~is formed with~~ includes a DRAM, and the other ~~is formed with~~ includes a flash memory.

9. (currently amended) The semiconductor device according to claim 6, wherein ~~the~~ a lower surface of said wiring substrate is formed with a plurality of bump electrodes constructing external connection terminals.

10. (new) The semiconductor device according to claim 1, wherein said microcomputer chip and said memory chip have respective terminals, a number of terminals of said microcomputer chip being much greater than a number of terminals of said memory chip.

11. (new) The semiconductor device according to claim 10, wherein the terminals of said memory chip are arranged such that they are not superposed over the terminals of said microcomputer chip in a plan view.

12. (new) The semiconductor device according to claim 7, wherein an under-fill resin is filled in a gap between said lower memory chip and said wiring substrate.